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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JOHNSTON, PHILLIP A	
ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 12/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,270	INANAMI ET AL.	
	Examiner	Art Unit	
	Phillip A Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 March 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

Claims Rejection – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, are rejected under 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 5,250,812 to Murai, in view of Watanabe, U.S. Patent No. 6,335,898.

Murai (812) discloses an electron beam lithography apparatus that includes an electron beam 22 emitted from an electron gun 21 is focused by a plurality of electron lenses 23 and 24 and deflected by deflection lenses 25 and 26 to irradiate a wafer 28 on a movable stage 27. The shape of the beam, is determined by two aperture plates, which include a first aperture plate 29 and a second aperture plate 210 Any aperture in the second aperture plate 210 is selected by electron beam shaping lense 211 to form any fixed shaped electron beam. Also, a rectangular aperture is provided at a central portion of the second aperture plate 210 so that a variable shaped beam is formed

according to conventional practice. See Column 3, line 63-68, and Column 4, line 1-10.

Murai (812) also discloses FIG. 3 is a flow chart for producing delineation data. First, LSI design data is given as CAD (computer aided design) data (step 31). The CAD data is stored in, for example, a memory 215. In general, the CAD data includes data of non-repetitive patterns (or random patterns) and data of repetitive patterns having unit patterns repeated at a coordinate and a pitch designated. In step 32, only the repetitive patterns are extracted from the CAD data. In step 33, a computer 213 (see FIG. 2) calculates the influence of a proximity effect in the pattern array on the basis of the CAD data. In the case where repeated unit patterns 41 have a high density, as shown in FIG. 4A, it is known that the proximity effect becomes uniform at the periphery of the pattern array 43. The computer 213 also determines the width of a periphery portion where the proximity effect is not uniform. A frame 44 shown in FIG. 4C represents a boundary of that periphery portion. In step 34, the computer 213 processes the repetitive pattern data to determine the shape and size of each of repeated unit patterns, which form an aperture and the number of the repeated unit patterns in the aperture in each of a longitudinal direction and a lateral direction. There may be the case where one pattern array to be delineated on the substrate includes a plurality of kinds of unit patterns. In that case, the above processing is performed for each unit pattern. Next or in step 36, the region 45 is delineated using the aperture determined in the above steps. Subsequently, the remaining region is delineated using a variable shaped beam (step 37). Thereafter, a memory capacitor forming step

and a wiring step were carried out, thereby completing the semiconductor device. The patterning for working of fine hole configurations was made by an electron beam lithography using an aperture plate of the present invention and the patterning at the other steps was made using a reduced projection lithography technique. See Column 4, line 14-15, and Column 5, line 6-13.

Murai (812) further discloses in FIG. 5A a region 51 delineated by a fixed shaped beam of 6.4 um square and a region 52 on the periphery portion delineated by a variable shaped beam. The region 52 delineated by the variable shaped beam requires 16 shots, as represented by numerals shown in patterns. On the other hand, in the region delineated by the fixed shaped beam, an area twice as large as the region 52 can be delineated by one shot. See Column 5, line 35-40. Also if the number of unit patterns to be formed in an aperture is selected to be 4X4 which is one sixteenth or in general l/m (m: natural number) of the number 64X64 of repeated unit patterns in the pattern array, 256 (=16X16) shots suffice for all of regions 63 or the whole of the pattern array. Namely, the delineation can be completed with the number of shots reduced to one fourth of that required in the case where the maximum size of beam is used. See Column 6, line 13-21.

It is implied herein, that the use of repeated unit patterns as taught by Murai (812), is equivalent to the "standard cell", as recited in Claims 1, 4 and 6, and the aperture containing the repeated unit patterns in accordance with Murai (812) is equivalent to the "Character Projection aperture", as recited in Claims 1,2,5, and 6.

Watanabe (898) discloses in FIG. 1 a storage device DB for data base in which the layout patterns and characteristics of a core circuit and a logic library are registered. The data base storage device DB is stored beforehand with data necessary for design including the layout patterns, specifications and characteristics of a plurality of memory cores MR which have different storage capacities and each of which has a multiplicity of data transmission lines, a group of modules for transfer circuit (or coupling circuit) TG which are set in conformity with the pitch of data transmission lines (or I/O lines) of the memory cores MR, respectively, and a logic library LL which includes basic gates for composing a logic circuit LC. A desired logic circuit LC can be easily composed from the logic library LL by use of a CAD tool for logic composition. See Column 5, line 57-68, and Column 6, line 1-12.

Hence, It would have been obvious to one of ordinary skill in the art, that the CAD data of Murais' (812) lithography exposure system can be modified to use the logic library data and composition process of Watanabe (898), making it possible to design projection exposures of an LSI chip promptly by selecting basic patterns from the libraries, composing a logic portion by use of a basic library for logic, and performing the placement and routing. Thereby reducing fabrication time.

3. Claims 7-21, are rejected under 35 U.S.C. 103(a), as being unpatentable over Murai (812), in view of Watanabe (898), and in further view of Shibata, U.S. Patent No. 5,371,373.

Shibata (373) discloses in FIG. 3, an LSI device pattern supplied from the LSI CAD/DA system 1 to an electron beam (EB) lithography data conversion system 2 as input data to be converted into data having such a format as readable by an EB lithography apparatus. If the input data represents such a repeated pattern (which is also called a cell in some LSI-CAD systems) as, for example, patterns of a memory device, then a cell projection lithography technique is utilized to perform efficient writing or delineating operation. In this case, the input data is processed by an EB lithography data generation system 3 of the cell projection lithography. The lithography data generated by the data conversion system 2 and the data generation system 3 (a lithography data generator and a pattern selector) is transferred to an EB lithography control system 4 and registered therein. See Column 4, line 24-39.

Shibata (373) further discloses in Figure 1, the operations executed by the EB lithography data conversion system 2 and the cell projection lithography data generation system 3. In step 49 LSI pattern data is read and input from the LSI-CAD/DA system 1. In the next step 50, the input data is classified into repetitive patterns or non-repetitive patterns based on the cell name and array structure of the input pattern data and previously temporarily registered. When the input data is classified as the repetitive patterns in step 50, the processing proceeds to step 51, where it is determined whether or not a cell projection condition 1 is satisfied. The cell projection condition 1 is such that the repetitive numbers of the repetitive patterns is sufficiently large . In step 52, the repetitive unit pattern mask is thus set and the

repetitive structure is simultaneously set, and then they are registered. Then, the processing proceeds to step 53, whereat the non-repetitive patterns temporally registered are extracted in step 50 and the extracted patterns are subjected to a normal lithography data conversion. In step 54, a preparing operation (mask layout and lithography data conversion) of the second transfer mask is carried out and the mask is set in the second transfer mask mechanism 20 in step 55.Then, the processing proceeds to step 56, where the mask and repetitive structure registered in step 52 are selected and composed with the lithography data of the non-repetitive pattern obtained in step 53. Next, the processing proceeds to step 57, where the lithography data obtained in step 56 is sorted according to the lithography sequence and output as lithography data. See Column 6, line 53-68, and Column 7, line 1-37.

As a result, it would have been obvious to one of ordinary skill in the art that the Murai (812) in view Watanabe (898), electron beam lithography system, can be modified to use a lithography control apparatus and method, to further reduce the number of lithography shots according to the teachings of Shibata (373), if so desired.

Conclusion

4. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (703) 305-7022. The examiner can normally be reached on Monday-Friday from 7:30 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee

can be reached at (703) 308-4116. The fax phone numbers are (703) 308-2864 and (703) 308-7721.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

PJ
December 10, 2002

BRUCE ANDERSON
PRIMARY EXAMINER